Secondary LDO Regulator Series for Local Power Supplies

500mA Secondary LDO Regulators for Local Power Supplies

Pb Free ROHM Electronic Components
RoHS Directive Compliance

BD□□KA5,BD□□KA5W Series,BD00KA5W Series

No.09024EAT01

●General Description

The BD□□KA5 series are low-saturation regulators that are available for output currents up to 500mA. The output voltage precision is ±1%. These secondary LDO regulators are offered in several output voltages and package lineups with or without ON/OFF switches (that set the circuit current to 0μA at shutdown). This series can be used for a broad spectrum of applications ranging from TVs and car audio systems to HDDs, PCs, and DVDs. There regulators have a built-in overcurrent protection circuit that prevents the destruction of the IC, due to output short circuits and a thermal shutdown circuit.

●Features

1) Maximum output current : 500mA
2) Output voltage precision : ±1%
3) Low-saturation voltage with PMOS output : 0.12V Typ.(Io=200mA)
4) Built-in over-current protection circuit
5) Built-in thermal shutdown circuit
6) Shutdown switch(BD□□KA5WFP and BD□□KA5WF series)
7) TO252-3,TO252-5 and SOP8 package lineup
8) Operating temperature range : -40℃ to +105℃
9) Ceramic capacitor compatible(recommended capacitance : 1μF or greater)

●Applications

Microcontrollers and all electronic devices that use logic circuits

●Product line up

Part Number	1.0	1.2	1.5	1.8	2.5	3.0	3.3	Variable	Package
BD□□KA5WFP	○	○	○	○	○	○	○	○	TO252-5
BD□□KA5WF	○	○	○	○	○	○	○	○	SOP8
BD□□KA5FP	○	○	○	○	○	○	○	−	TO252-3

Part Number：BD□□KA5□□
a b c

Symbol	Details			
a	Output Voltage Designation			
	□□	Output Voltage(V)	□□	Output Voltage(V)
	10	1.0V(Typ.)	25	2.5V(Typ.)
	12	1.2V(Typ.)	30	3.0V(Typ.)
	15	1.5V(Typ.)	33	3.3V(Typ.)
	18	1.8V(Typ.)	00	Variable Output Typ
b	Switch "W" included：Built-in shutdown switch "W" not included：No shutdown switch			
c	Package FP：TO252-5 / TO252-3 F：SOP8			

●Absolute Maximum Ratings(Ta=25℃)

Parameter		Symbol	Limits	Unit.
Power Supply Voltage		Vcc	-0.3～+7.0 *1	V
Output Control Terminal Voltage		V_{CTL}	-0.3～Vcc *1	V
Power Dissipation	TO252-3	Pd	1200 *2	mW
	TO252-5		1300 *3	
	SOP8		687.6 *4	
Operating Temperature Range		Topr	-40～+105	℃
Ambient Storage Temperature		Tstg	-55～+150	℃
Maximum Junction Temperature		Tjmax	150	℃

*1 Must not exceed Pd
*2 When a 70mm×70mm×1.6mm glass epoxy board is used. Reduce by 9.6 mW/℃ over 25℃.
*3 When a 70mm×70mm×1.6mm glass epoxy board is used. Reduce by 10.4mW/℃ over 25℃.
*4 When a 70mm×70mm×1.6mm glass epoxy board is used. Reduce by 5.5 mW/℃ over 25℃.

●Recommended Operating Range (Ta=25℃)

Parameter	Symbol	Min.	Max.	Unit.
Input Power Supply Voltage	Vcc	2.3	5.5	V
Output Current	Io	0	500	mA
Output Voltage Configuration Range *5	Vo	1.0	4.0	V
Output Control Terminal Voltage	V_{CTL}	0	Vcc	V

*5 Only BD00KA5WFP and BD00KA5WF

●Electrical Characteristics (abridged)

BD□□KA5WFP / WF / FP
(Unless specified otherwise,Ta=25℃,V_{CTL}=2V,Vcc=2.5V(Vo=1.0V,1.2V,1.5V,1.8V),Vcc=3.3V(Vo=2.5V),Vcc=5.0V(Vo=3.0V,3.3V))

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Conditions
Output Voltage	Vo	Vo(T)-0.015	Vo(T)	Vo(T)+0.015	V	Io＝200mA (Vo=1.0V,1.2V)
		Vo(T)×0.99	Vo(T)	Vo(T)×1.01	V	Io＝200mA (Vo≧1.5V)
Circuit Current at Shutdown	Isd	-	0	1	μA	V_{CTL} =0V,Io=0mA (during OFF mode)
Minimum I/O Voltage Difference *6	ΔVd	-	0.12	0.20	V	Io=200mA,Vcc=0.95×Vo
Output Current Capacity	Io	500	-	-	mA	
Input Stability *7	Reg.I	-	10	35	mV	Vcc=Vo+0.5V→5.5V,Io=200mA
Load Stability	Reg.L	-	25	75	mV	Io=0mA→500mA
Output Voltage Temperature Coefficient *8	Tcvo	-	±100	-	ppm/℃	Io=5mA,Tj=0～125℃

Vo(T) : Preset output voltage value
*6 When Vo≧2.5V
*7 When 1.0≦Vo≦1.8V, Vcc=2.3V→5.5V
*8 Design guarantee(100% shipping inspection not performed)

BD00KA5WFP / WF
(Unless specified otherwise, Ta=25℃, Vcc=2.5V,VL＝2V,R1=30kΩ,R2=30kΩ *9)

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Conditions
Circuit Current at Shutdown	Isd	-	0	1	μA	V_{CTL} =0V, Io=0mA (during OFF mode)
Reference Voltage	V_{ADJ}	0.742	0.750	0.758	V	Io=50mA
Minimum I/O Voltage Difference*10	ΔVd	-	0.12	0.20	V	Io=200mA,Vcc=0.95×Vo
Output Current Capacity	Io	500	-	-	mA	
Input Stability	Reg.I	-	10	35	mV	Vcc=Vo+0.5V→5.5V,Io=200mA
Load Stability	Reg.L	-	25	75	mV	Io=0mA→500mA
Output Voltage Temperature Coefficient *11	Tcvo	-	±100	-	ppm/℃	Io=5mA,Tj=0～125℃

*9 VOUT=VADJ×(R1+R2)÷R1(V)
VADJ×0.75V(Typ.)
*10 When Vo≧2.5V
*11 Design guarantee(100% shipping inspection not performed)

●**Reference Data (Unless specified otherwise, Vcc=25V,V_{CTL} =2V,and Io=0mA)**

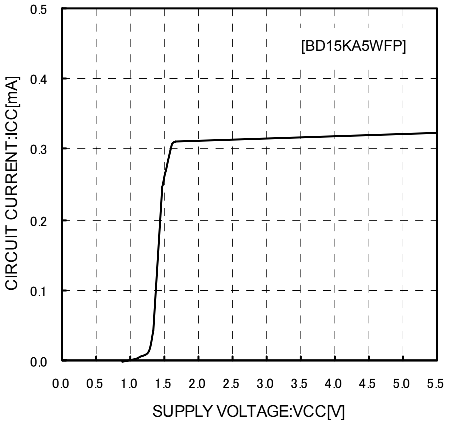


Fig.1 Circuit current

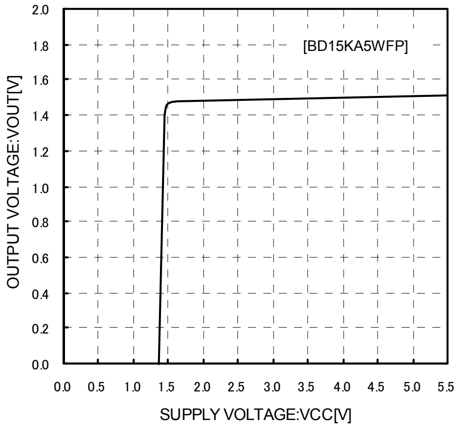


Fig.2 Input Stability (Io=0mA)

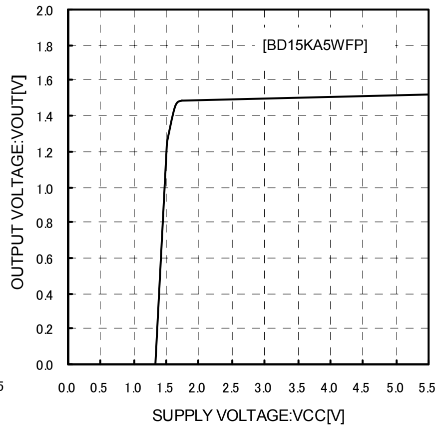


Fig.3 Input Stability (Io=500mA)

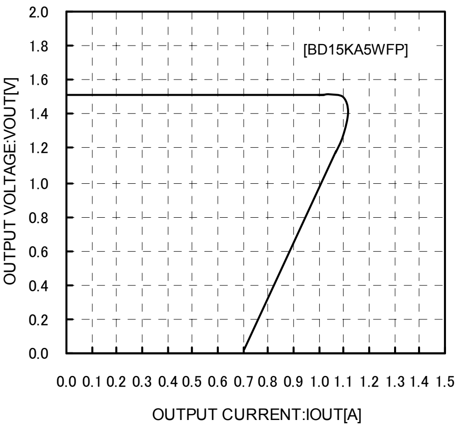


Fig.4 Load Stability

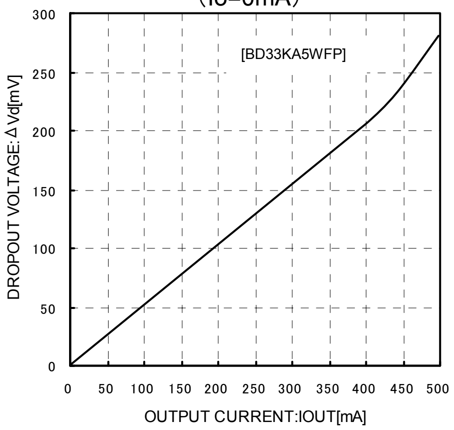


Fig.5 Input/Output Voltage Difference (Vcc=3.135V)

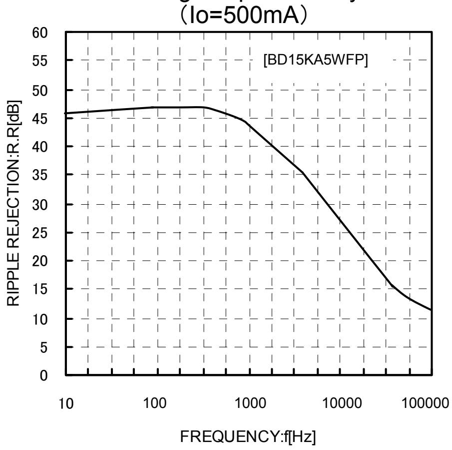


Fig.6 Ripple Rejection (ein=10dBV,Io=100mA)

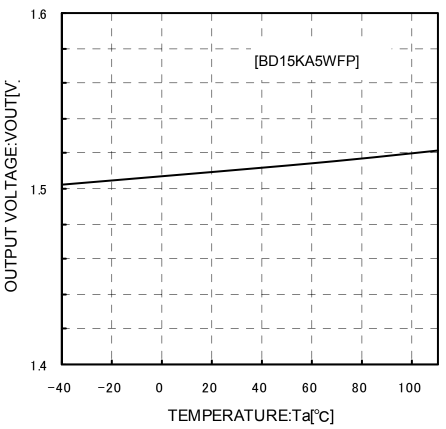


Fig.7 Output Voltage (Io=5mA)

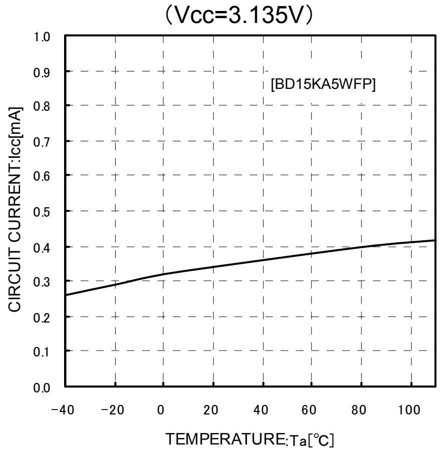


Fig.8 Circuit Current Temperature Characteristics

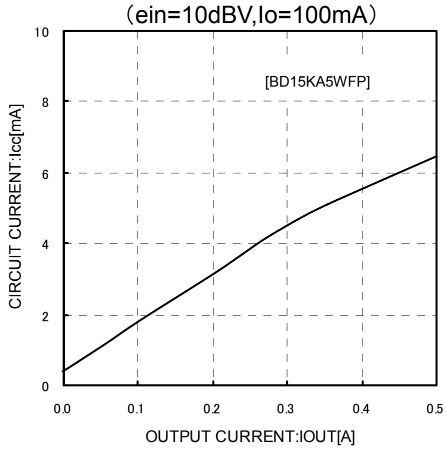


Fig.9 Circuit Current by load Level

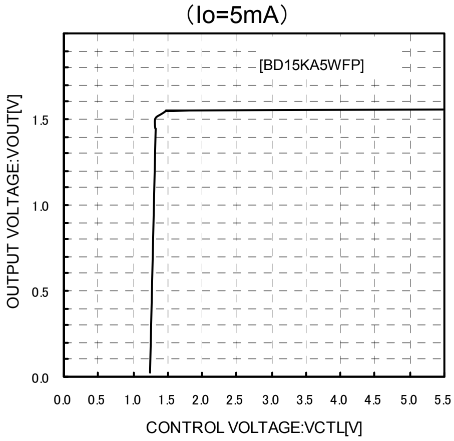


Fig.10 CTL Voltage vs. Output Voltage

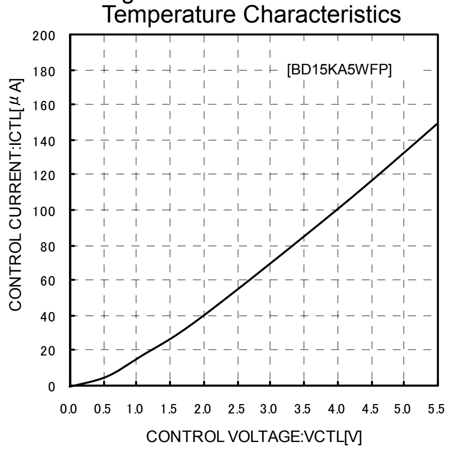


Fig.11 CTL Voltage vs. Output Current

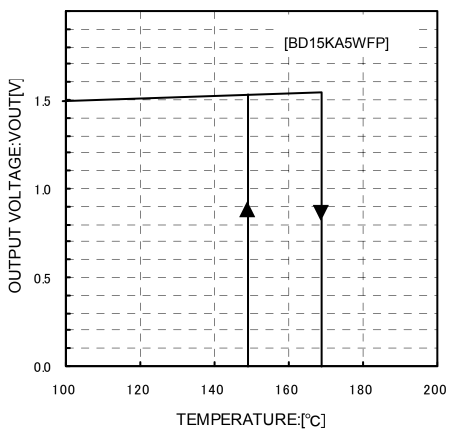


Fig.12 Thermal Shutdown Circuit Characteristics (Io=5mA)

●Block diagrams, Standard circuit examples

[BD00KA5WFP]

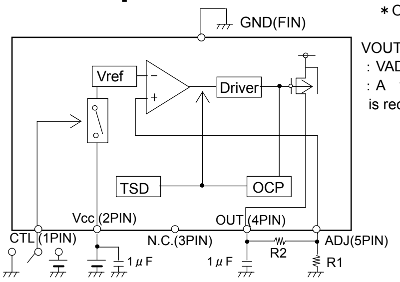
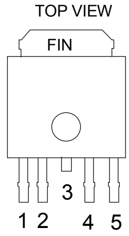


Fig.13

＊Output voltage configuration

VOUT=VADJ×（R1+R2）÷R1(V)
: VADJ=0.75V(Typ.)
: A value of approximately 30kΩ is recommended for R1.



TO252-5(BD00KA5WFP)

Pin No.	PinName	Function
1	CTL	Output voltage ON/OFF control
2	Vcc	Power supply voltage input
3	N.C.	Unconnected terminal
4	OUT	Voltage output
5	ADJ	Output voltage configuration terminal
FIN	GND	GND

[BD□□KA5WFP]

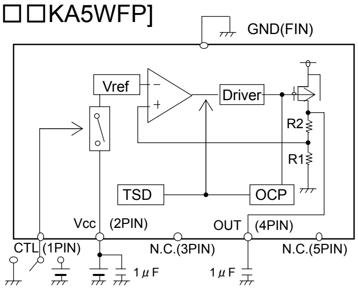
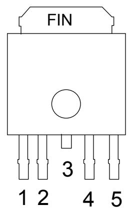


Fig.14



TO252-5(BD□□KA5WFP)

Pin No.	Pin Name	Function
1	CTL	Output voltage ON/OFF control
2	Vcc	Power supply voltage input
3	N.C.	Unconnected terminal
4	OUT	Voltage output
5	N.C.	Unconnected terminal
FIN	GND	GND

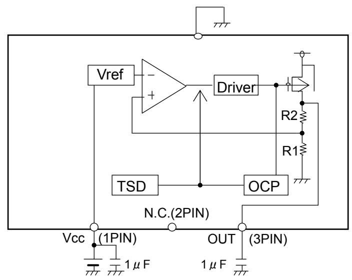
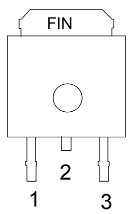


Fig.15



TO252-5(BD□□KA5FP)

Pin No.	Pin Name	Function
1	Vcc	Power supply voltage input
2	N.C.	Unconnected terminal
3	OUT	Voltage output
FIN	GND	GND

[BD00KA5WF]

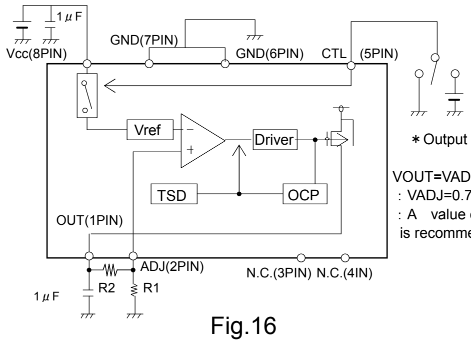
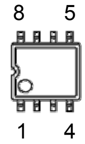


Fig.16

＊Output voltage configuration

VOUT=VADJ×（R1+R2）÷R1(V)
: VADJ=0.75V(Typ.)
: A value of approximately 30kΩ is recommended for R1.



SOP8(BD00KA5WF)

Pin No.	Pin Name	Function
1	OUT	Voltage output
2	ADJ	Output voltage configuration terminal
3	N.C.	Unconnected terminal
4		
5	CTL	Output voltage ON/OFF control
6	GND	GND
7		
8	Vcc	Power supply voltage input

[BD□□KA5WF]

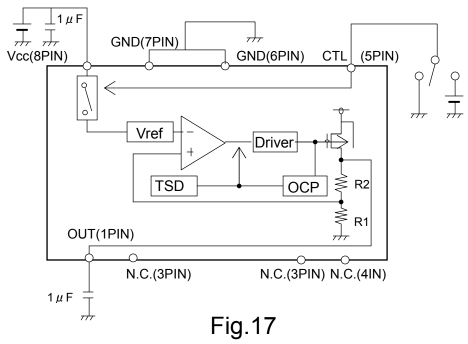
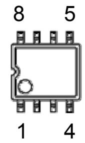


Fig.17



SOP8(BD□□KA5WF)

Pin No.	Pin Name	Function
1	OUT	Voltage output
2	N.C.	Unconnected terminal
3		
4		
5	CTL	Output voltage ON/OFF control
6	GND	GND
7		
8	Vcc	Power supply voltage input

N.C. pins are electrically open to the inside of the IC chip.

●Input / Output Equivalent Circuit Diagrams

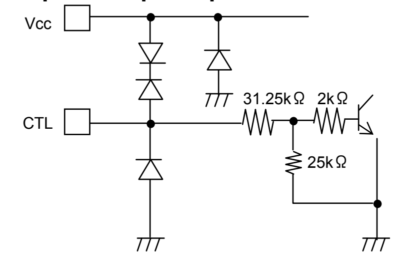


Fig.18

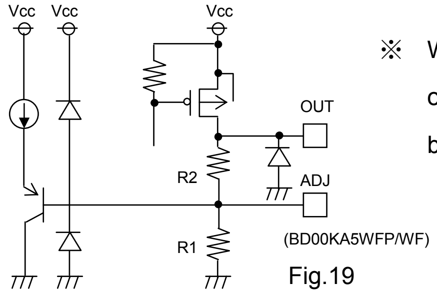


Fig.19

※ With BD00KA5WFP/WF,R1and R2 are connected outside the IC between ADJ and GND and between OUT and ADJ.

●Thermal Design

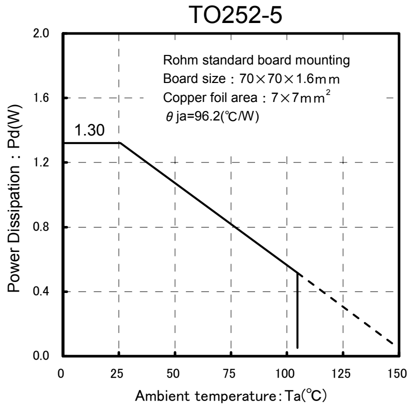


Fig.20 Power Dissipation heat reducing characteristics

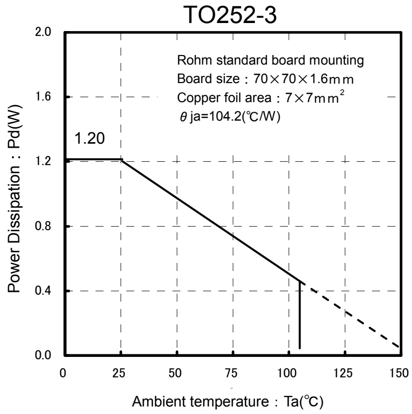


Fig.21 Power Dissipation heat reducing characteristics

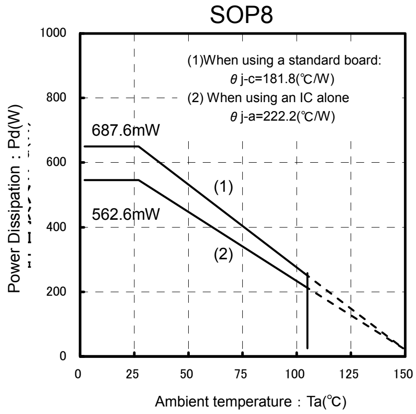


Fig.22 Power Dissipation heat reducing characteristics

When using at temperatures over Ta=25℃, please refer to the power dissipation shown in Fig.20 through 22.
The IC characteristics are closely related to the temperature at which the IC is used, so if the temperature exceeds the maximum junction temperature Tj_{MAX}, the device may malfunction or be destroyed. The heat of the IC requires sufficient consideration regarding instantaneous destruction and long-term operation reliability. In order to protect the IC from thermal damage, it is necessary to operate it at temperatures less than the maximum junction temperature Tj_{MAX}.
Even when the ambient temperature Ta is a normal temperature(25℃), the chip(junction) temperature Tj may be quite high, so please operate the IC at temperatures less than the acceptable loss Pd.

The calculation method for power consumption Pc(W) is as follows :

$$Pc = (Vcc-Vo)\times Io+Vcc\times Icca$$

$$\text{Acceptable loss } Pd \geqq Pc$$

Solving for the load current IO in order to operate within the acceptable loss,

Vcc : Input voltage
Vo : Output voltage
Io : Load current
Icca : Circuit current

$$Io \leqq \frac{Pd - Vcc\times Icca}{Vcc-Vo}$$

It is then possible to find the maximum load current Io_{MAX} with respect to the applied voltage Vcc at the time of thermal design.

Calculation Example

Example 1) When Ta=85℃, Vcc=2.5V, Vo=1.0V

$$Io \leqq \frac{0.676-2.5\times Icca}{2.5-1.0}$$

$$Io \leqq 440mA \text{ (Icca : 2mA)}$$

BA10KA5WFP（TO252-5 packaging）
θja=96.2℃/W → -10.4mW/℃
25℃=1300mW → 85℃=676mW

Please refer to the above information and keep thermal designs within the scope of acceptable loss for all operating temperature ranges.
The power consumption PC of the IC when there is a short circuit (short between Vo and GND) is :

$$Pc=Vcc\times(Icca+Ishort)$$

*Ishort : Short circuit current

●Terminal Vicinity Settings and Cautions

・Vcc Terminal

Please attach a capacitor (greater than 1 μF) between Vcc and GND.
The capacitance values differ depending on the application, so chose a capacitor with sufficient margin and verify the operation on actual board.

・GND Terminal

Please be sure to keep the set ground and IC ground at the same potential level so that a potential difference does not arise between them. If a potential difference arises between the set ground and the IC ground, the preset voltage will not be output properly, causing the system to become unstable. Please reduce the impedance by making the ground patterns as wide as possible and reducing the distance between the set ground and the IC ground as much as possible.

・CTL Terminal

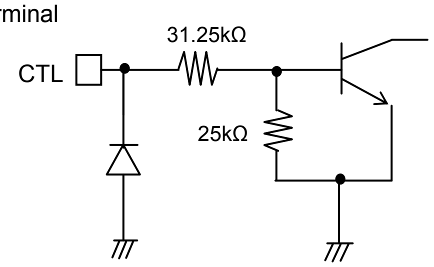


Fig.23 Input equivalent circuit

The CTL terminal is turned ON at 2.0V and higher, and OFF at 0.8V and lower, within the operating power supply voltage range.The power supply and the CTL terminal may be started up and shut down in any order without problems.

●Vo Terminal

Please be sure to attach an anti-oscillation capacitor between V_o and GND.

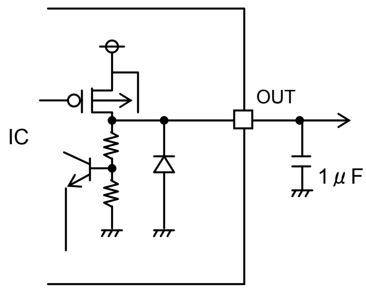


Fig.24 Output Equivalent Circuit

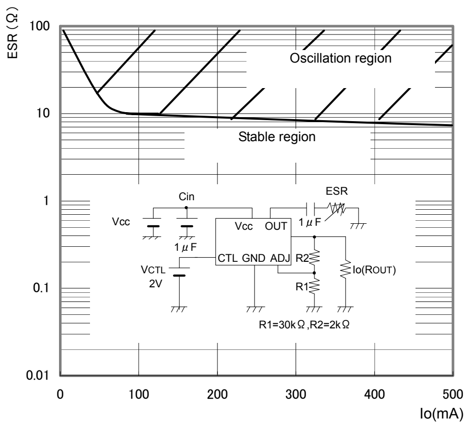
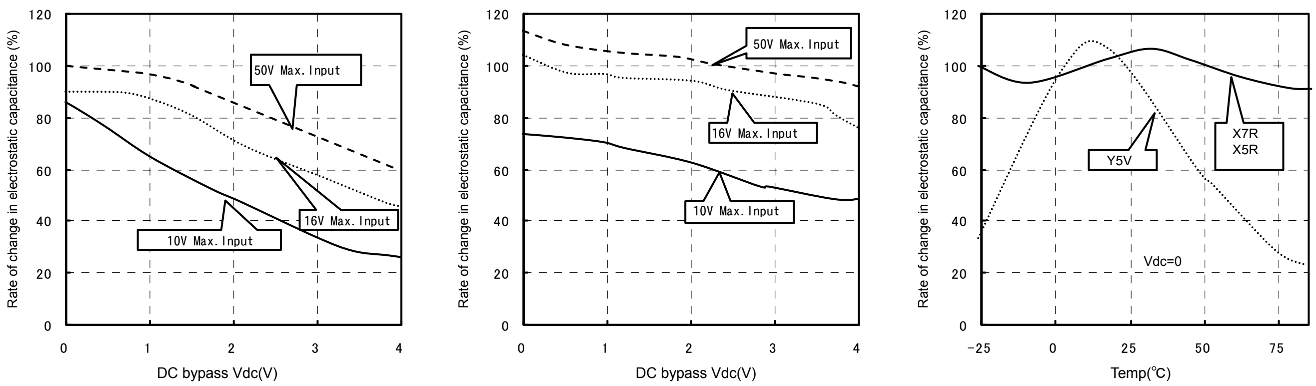


Fig.25 ESR-Io Characteristics

Be sure to place an anti-oscillation capacitor between the output terminal and the GND. Oscillations may arise if the capacitance value changes, due to factors such as temperature changes. A 1 μF capacitor with small internal series resistance (ESR) such as a ceramic capacitor is recommended as an anti-oscillation capacitor. Ceramic capacitors generally have favorable temperature characteristics and DC bypass characteristics. When selecting a ceramic capacitor, a high voltage capacitor (good DC bypass characteristics) with temperature characteristics that are superior to those of X5R or X7R, is recommended. In applications where input voltage and load fluctuations are rapid, please decide on a capacitor after sufficiently confirming its properties according to its specifications in the actual application.



(a) Capacitance-bypass characteristics (Y5V)

(b) Capacitance-bypass characteristics (X5R,X7R)

(C) Capacitance-temperature characteristics (X5R,X7R,Y5V)

Fig.26 :General characteristics of ceramic capacitors

●Other Caution

○Protection Circuits

Over-current Protection Circuit

A built-in over-current protection circuit corresponding to the current capacity prevents the destruction of the IC when there are load shorts. This protection circuit is a “7”-shaped current control circuit that is designed such that the current is restricted and does not latch even when a large current momentarily flows through the system with a high-capacitance capacitor. However, while this protection circuit is effective for the prevention of destruction due to unexpected accidents, it is not suitable for continuous operation or transient use. Please be aware when creating thermal designs that the over-current protection circuit has negative current capacity characteristics with regard to temperature.

○Thermal Shutdown Circuit (Thermal Protection)

This system has a built-in temperature protection circuit for the purpose of protecting the IC from thermal damage. As shown in Fig. 20-22, this must be used within the range of acceptable loss, but if the acceptable loss is continuously exceeded, the chip temperature Tj increases, causing the thermal shutdown circuit to operate. When the thermal shutdown circuit operates, the operation of the circuit is suspended. The circuit resumes operation immediately after the chip temperature Tj decreases, so the output repeats the ON and OFF states (Please refer to Figs.12 for the temperatures at which the temperature protection circuit operates).
There are cases in which the IC is destroyed due to thermal runaway when it is left in the overloaded state. Be sure to avoid leaving the IC in the overloaded state.

○Reverse Current

In order to prevent the destruction of the IC when a reverse current flows through the IC, it is recommended that a diode be placed between the Vcc and Vo and a pathway be created so that the current can escape (Refer to Fig.27).

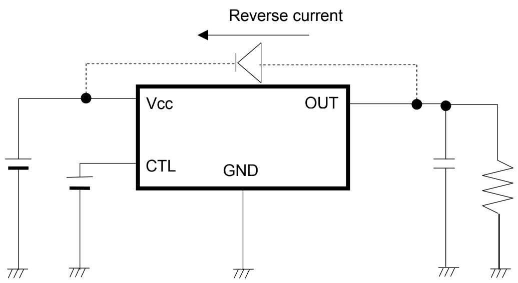


Fig.27 : Bypass diode

○This IC is BI-CMOS IC that has a P-board (substrate) and P+ isolation between each element, as shown in Fig.28. A P-N junction is formed between this P-layer and the N-layer of each element, and the P-N junction operates as :

- a parasitic diode when the electric potential relationship is GND> Terminal A, GND> Terminal B, or
- a parasitic transistor when the electric potential relationship is Terminal B > GND> Terminal A.

Parasitic elements are structurally inevitable in the IC. The operation of parasitic elements induces mutual interference between circuits, causing malfunctions and eventually the destruction of the IC. Take precaution as not to use the IC in ways that would cause parasitic elements to operate. For example, applying a voltage that is lower than the GND (P-board) to the input terminal.

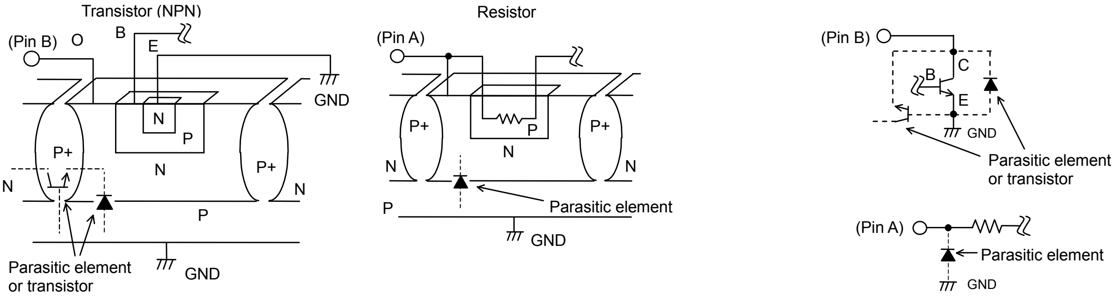


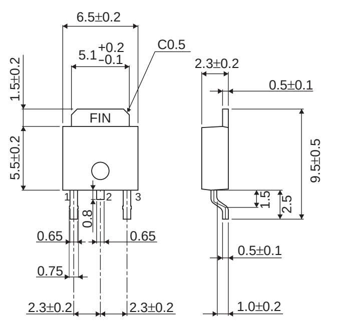
Fig. 28 : Basic structure example

●**Ordering part number**

B D 1 8 K A 5 W F P - E 2

- Part number: B D
- Output voltage: 1 8 — 00:Variable, Other:Fixed
- Current capacity: K A 5 — 500mA
- Shutdown switch: W — W : Include
- パッケージ: F P — FP : TO252-3, TO252-5; F : SOP8
- Packaging and forming specification: E 2 — E2: Embossed tape and reel

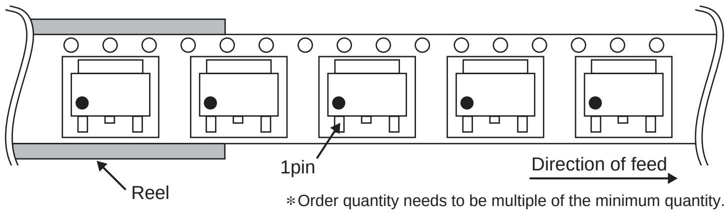
TO252-3



(Unit : mm)

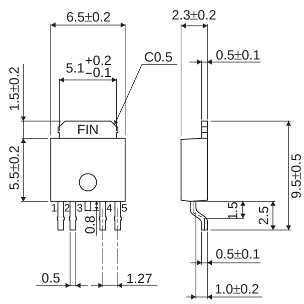
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

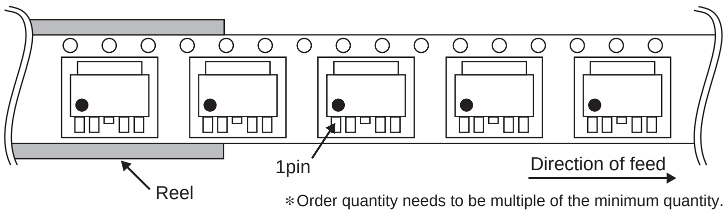
TO252-5



(Unit : mm)

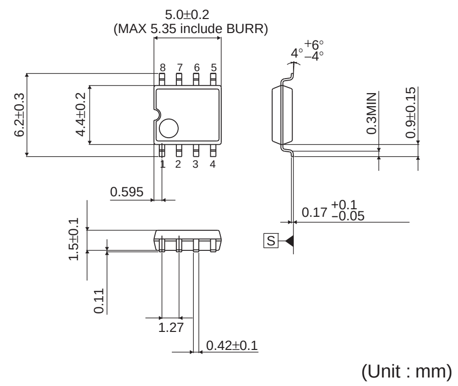
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand)



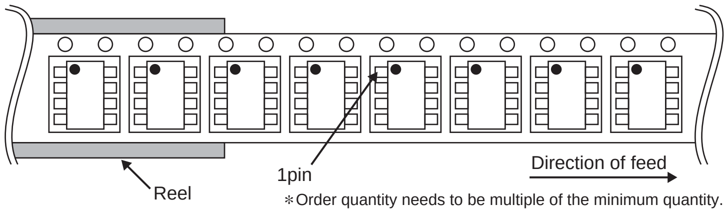
※Order quantity needs to be multiple of the minimum quantity.

SOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

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